## IN THE DRAWINGS

Corrected drawings are supplied herewith, each labeled as "REPLACEMENT SHEET". The cross-hatching has been corrected in each of the Figures.

## REMARKS

This paper responds to the Office Action mailed on November 15, 2005. Claims 40-58 are pending in this application.

*Drawing Objections*

The Examiner objects to the figures because of improper cross-hatching. Applicant provides herewith Replacement Sheets with the cross-hatching corrected.

*First §102 Rejection of the Claims*

Claims 40, 42 and 44 were rejected under 35 USC § 102(b) as being anticipated by Kumar (U.S. 5,227,013). A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *M.P.E.P. ' 2131.* To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. V. Guardian Industries Corp.*, 75 F.3d 1558, 37 USPQ2d 1618 (Fed. Cir. 1996). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

As part of making the rejection, the Examiner states at pages 3-4 of the Office Action that

> "Kumar, in figure 6, discloses a substrate comprising: . . . a second conductive layer (34) between the second dielectric layer and the third dielectric layer, the second conductive layer including a first skip via (V1, as marked on figure 6 in appendix "C") that extends through the first and second dielectric layers; . . ."

Applicant respectfully traverses these assertions. Applicant respectfully notes that FIGS. 7 and 8 of Kumar would have been more appropriately marked up by the Examiner because the marked up FIGS. 6E and 6 F do not include any vias.

Applicant respectfully directs the Examiner's attention to FIGS. 7 and 8 of Kumar which show that the second conductive layer 34 does not include any vias. Applicant notes that each of vias is shown as a separate entity from the second conductive layer 34. Therefore, Kumar does

not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" as recited in claim 40.

Reconsideration and allowance of claims 40, 42 and 44 are respectfully requested.

*Second §102 Rejection of the Claims*

Claims 47-49 and 51 were rejected under 35 USC § 102(b) as being anticipated by Kumar (U.S. 5,227,013). As part of making the rejection, the Examiner states at pages 4-5 of the Office Action that

> "Kumar, in Figure 6F, discloses a substrate comprising: . . . a second conductive layer (conductive layer between the dielectric layer 36 and 30) between the second and third dielectric layers, the second conductive layer including a first skip via (V1, as marked on figure 6F in appendix "D" that extends through the first and second dielectric layers; a fourth dielectric layer (14), the third dielectric layer being between the second and fourth dielectric layers; a third conductive layer (conductive layer between the dielectric layers 30 and 40) between the third and fourth dielectric layers; and a fourth conductive layer (conductive layer on dielectric layer 14) on the fourth dielectric layer, the fourth conductive layer including a second skip via (V2, as marked on figure 6F in appendix "D") that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another (see marked up figure 6F)."

Applicant respectfully traverses these assertions. Applicant again respectfully notes that FIGS. 7 and 8 of Kumar would have been more appropriately marked up by the Examiner because the marked up FIGS. 6E and 6F do not include any vias.

Applicant respectfully directs the Examiner's attention to FIGS. 7 and 8 of Kumar which show that the second conductive layer (cited by the Examiner as the conductive layer between the dielectric layers 36, and 30) does not include any vias. Applicant notes that each of the vias is shown as a separate entity from the second conductive layer cited by the Examiner. Therefore, Kumar does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" as recited in claim 47.

Reconsideration and allowance of claims 47-49 and 51 are respectfully requested.

*Third §102 Rejection of the Claims*

Claims 40-44 were rejected under 35 USC § 102(e) as being anticipated by Carpenter et al. (U.S. 6,810,583). As part of making the rejection, the Examiner states at page 6 of the Office Action that

> "Carpenter, in figure 6, discloses a substrate comprising: . . . a second conductive layer (C2 , as marked up on figure 6 in appendix "A"); between the second dielectric layer and the third dielectric, the second conductive layer including a first skip via (57) that extends through the first and second dielectric layers; and a third conductive layer (C3) on the third dielectric layer, the third conductive layer including a second via (26) that extends through the third dielectric layer, the second via and the first skip via being stacked on to of one another (see marked up figure 6 in appendix "A")."

Applicant respectfully traverses these assertions. Applicant respectfully refers to the Examiner's marked up drawing which shows that the layer C2 (indicated by the Examiner as the second conductive layer) does not include any vias. Applicant notes that each of the vias is shown as a separate entity from the marked C2 layer. Therefore, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" as recited in claim 40.

Applicant also respectfully refers to the Examiner's marked up drawing which shows that the layer C3 (indicated by the Examiner as the third conductive layer) does not include any vias. Applicant notes that each of the vias is shown as a separate entity from the marked C3 layer. Therefore, Carpenter does not teach or suggest "the third conductive layer including a second via that extends through the third dielectric layer" as recited in claim 40.

Reconsideration and allowance of claims 40- 44 are respectfully requested.

*Fourth §102 Rejection of the Claims*

Claims 47-51 were rejected under 35 USC § 102(e) as being anticipated by Carpenter et al. (U.S. 6,810,583). As part of making the rejection, the Examiner states at pages 7-8 of the Office Action that

> "Carpenter, in figure 7, discloses a substrate comprising: . . . a second conductive layer (C3, marked up on figure 7 in appendix "B") between the second and third dielectric layers, the second conductive layer including a first skip via (VI, marked up on figure 7 in appendix "B") that extends through the

> first and second dielectric layers; a fourth dielectric layer (D4, marked up on figure 7 in appendix "B"), the third dielectric layer being between the second and fourth dielectric layers; a third conductive layer (C4, marked up on figure 7 in appendix "B") between the third and fourth dielectric layers; and a fourth conductive layer (C5, marked up on figure 7 in appendix "B") on the fourth dielectric layer, the fourth conductive layer including a second skip via (V2, marked up on figure 7 in appendix "B") that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another (see marked figure 7 in appendix "B")."

Applicant respectfully traverses these assertions. Applicant respectfully refers to the Examiner's marked up figure 7 which shows that the layer C3 (indicated by the Examiner as the second conductive layer) does not include any vias. Applicant notes that each of the vias is shown as separate entities from the marked C3 layer. Therefore, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" as recited in claim 47.

Applicant also respectfully refers to the Examiner's marked up figure 7 which shows that the layer C5 (indicated by the Examiner as the fourth conductive layer) does not include any vias. Applicant notes that each of the vias is shown as a separate entity from the marked C5 layer. Therefore, Carpenter does not teach or suggest "the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers" as recited in claim 47.

Reconsideration and allowance of claims 47-51 are respectfully requested.

*First §103 Rejection of the Claims*

Claims 54-56 were rejected under 35 USC § 103(a) as being unpatentable over Carpenter et al. The references must teach or suggest all the claim elements. M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). As part of making the rejection, the Examiner states at pages 9-10 of the Office Action that "Carpenter discloses all the features of the claimed invention as applied to claim 47 above, . . ."

Applicant respectfully traverses this assertion. As discussed above, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" or "the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers" as recited in claim 47. Claims 54-56

depend from claim 47 such that claims 54-56 incorporate all of the limitations of claim 47. Therefore, claims 54-56 are allowable for the reasons provided above with regard to claim 47.

The Examiner further states at page 10 of the Office Action that

> "It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with the third skip via connected to the sixth conductive layer, in order to have desired electric connection for signal, power or ground."

Applicant respectfully traverses this assertion and notes that the cited reference has no teaching or suggestion as to any of the conductive layers including a via.

Reconsideration and allowance of claims 54-56 are respectfully requested.

*Second §103 Rejection of the Claims*

Claims 45, 46, 52, 53, 57 and 58 were also rejected under 35 USC § 103(a) as being unpatentable over Carpenter et al. and further in view of Uchikawa et al. (U.S. 6,531,661) and Asai et al. (U.S. 6,534,723).

*Claims 45-46*

As part of making the rejection, the Examiner states at page 11 of the Office Action that "Carpenter discloses all the features of the claimed invention as applied to claim 40 above." Applicant respectfully traverses this assertion. As discussed above, Carpenter does not teach or suggest "the second conductive layer including a first skip via that extends through the first and second dielectric layers" or "the third conductive layer including a second via that extends through the third dielectric layer" as recited in claim 40. Claims 45-46 depend from claim 40 such that claims 45-46 incorporate all of the limitations of claim 40. Since Uchikawa et al. and Asai also do not appear to include these limitations, claims 45-46 are allowable for the reasons provided above with regard to claim 40.

*Claims 52, 53, 57 and 58*

The Examiner further states at page 13 of the Office Action that "Carpenter discloses all the features of the claimed invention as applied to claim 47 above, . . ." Applicant respectfully traverses this assertion. As discussed above, Carpenter does not teach or suggest "the second

conductive layer including a first skip via that extends through the first and second dielectric layers" or "the fourth conductive layer including a second skip via that extends through the third and fourth dielectric layers" as recited in claim 47. Claims 52, 53, 57 and 58 depend from claim 47 such that claims 52, 53, 57 and 58 incorporate all of the limitations of claim 47. Since Uchikawa et al. and Asai also do not appear to include these limitations, claims 52, 53, 57 and 58 are allowable for the reasons provided above with regard to claim 47.

Reconsideration and allowance of claims 52, 53, 57 and 58 are respectfully requested.

*Traversal of Pending 35 USC § 102 & 103 rejections*

Applicant respectfully traverses each of the pending 35 USC § 102 & 103 rejections. Applicant also respectfully reserves the right to traverse any statements that were made in the Office Action relating to the rejections (e.g., under MPEP 2144.04 among other things). Applicant is expressly not admitting to any assertions made in the Office Action.

*Reservation of Right to Swear Behind References*

Applicant reserves the right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

*Conclusion*

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Andrew Peret at 262-646-7009, or the below-signed attorney at 612-349-9592, to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

DAISUKE KAWAGOE

By his Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 349-9592

Date Jan. 17, 2006

By Ann M. McCrackin
Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 17th day of January 2006.

Amy Moriarty

Name

Signature